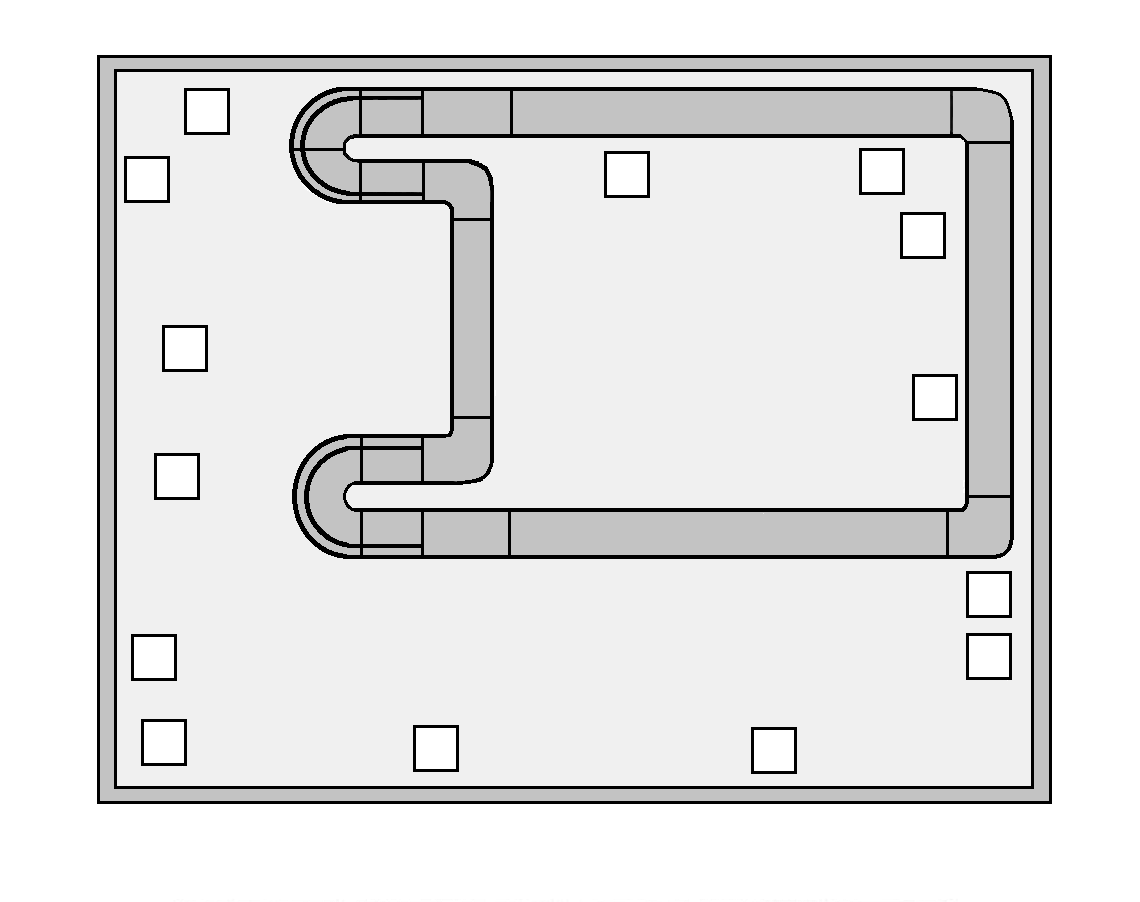
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**2110**

**2113**

**REV01**

IRS2110\_REV00

IRS2113\_REV00

**MASK**

**REF**

**VSS**

**VD**

**DZ**

**VDD**

**HIN**

**SD**

**LIN**

**LO**

**COM**

**VCC**

**VC**

**CZ**

**VS**

**VBZ**

**VB**

**HO**

NOTE:

Both VCC and VCCZ should be connected

Both VDD and VDDZ should be connected

Both VB and VBZ should be connected

**.071”**

**.075”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0039” X .0039”**

**Backside Potential: FLOATING**

**Mask Ref: IRS2110 / IRS2113**

**APPROVED BY: DK DIE SIZE .071” X .075” DATE: 8/30/21**

**MFG: INT’L RECTIFIER THICKNESS .029” P/N: IRS2110**

**DG 10.1.2**

#### Rev B, 7/1